What is claimed is:

1. A memory card comprising:

a memory chip, and

a controller connected to the memory chip, having a buffer storing data temporarily, and transferring data between outside and the memory chip via said buffer,

wherein, in a first operation mode, the controller clears the data stored in the buffer when said data in the buffer is transferred to the memory chip, and in a second operation mode, the controller does not clear the data stored in the buffer when said data in the buffer is transferred to the memory chip.

2. The memory card according to claim 1,

wherein the controller transfers the data in the buffer to the memory chip in response to a write command input from outside.

3. The memory card according to claim 1,

wherein the controller comprises a buffer clear register in which the first operation mode or the second operation mode is set, and said buffer clear register is settable from outside.

4. The memory card according to claim 1,

wherein the controller comprises a transfer circuit which transfers the data in the buffer to the memory chip,

and said transfer circuit transfers to the memory chip the data in the buffer without reversing the data in case of a non-reverse mode, or said transfer circuit transfers to the memory chip data produced by reversing the data in the buffer in case of a reverse mode.

5. The memory card according to claim 4,

wherein the controller comprises an inversion register in which the reverse mode or the non-reverse mode is set, and said inversion register is settable from outside.

6. The memory card according to claim 1,

wherein the number of external terminals provided in the controller is less than the number of connection terminals connecting the controller to the memory chip.

7. A test method for a memory card having a memory chip, and a controller which is connected to said memory chip, has a buffer storing data temporarily, and transfers data between outside and the memory chip via said buffer, said test method comprising:

a storage step including inputting a predetermined write data into the memory card, and storing the write data into the buffer; and

a write step including inputting write addresses and write commands repeatedly into the memory card, and writing the write data stored in the buffer into an area designated

by the write addresses in the memory chip,

wherein, in the write step, a non-clearance mode is set in which the write data stored in the buffer is not cleared when the write data is transferred to the memory chip.

8. The memory card test method according to claim 7,

wherein the write step is repeatedly executed for a plurality of times after one execution of the storage step.

9. A test method for a memory card having a memory chip, and a controller which is connected to said memory chip, has a buffer storing data temporarily, and transfers data between outside and the memory chip via said buffer, said test method comprising:

a storage step including inputting a predetermined write data into the memory card, and storing the write data into the buffer;

a first write step including inputting write addresses of a first group and write commands into the memory card, and writing the write data stored in the buffer into an area designated by the write addresses of the first group in the memory chip without reversing the write data; and

a second write step of inputting write addresses of a second group and write commands into the memory card, and writing data produced by reversing the write data stored in the buffer into an area designated by the write addresses

of the second group in the memory chip,

wherein, in the write steps, a non-clearance mode is set, in which the write data stored in the buffer is not cleared when the write data is transferred to the memory chip.

10. The memory card test method according to claim 9,

wherein the first write step and the second write step are alternately executed in repetition.

11. The memory card test method according to claim 9,

wherein the first write step is consecutively executed in repetition, and the second write step is consecutively executed in repetition.

12. The memory card test method according to claim 9,

wherein, in the first write step, the controller is set in a non-reverse mode, and in the second write step, the controller is set in a reverse mode.